University of Stuttgart
Institute of Smart Sensors

Master thesis
Design and Implementation of a Semi-Digital PLL

The detection of electron paramagnetic resonance (EPR) signals using LC oscillators (Fig. 1, left) has recently gained significant attention in the research community as a tool to realize portable, yet high-performance EPR spectrometers. In order to precisely control the phase of the oscillator from an external reference, semi-digital (SD) PLLs (Fig. 1 right) are promising candidates for several reasons. However, such dual-path PLLs generally require a high gain proportional path (P-path) to ensure stability. The usual way to implement the P-Path is through a resetting charge pump. This however, introduces spurs and increases the RMS error of the generated frequency sequence.

In this thesis, you will analyze and modify the architecture of a conventional SD PLL to tackle the above-mentioned problems. You will start by reviewing the mathematical model followed by system-level simulations in Matlab. You will finally implement the resulting modified architecture on schematic-level in Cadence Virtuoso.

Requirements:

- ✓ Basic knowledge in analog circuit design and control theory.
- ✓ Basic knowledge of Matlab and Cadence.

Duration: 6 months

Contact person: **Khubaib Khan**, khubaib.khan@iis.uni-stuttgart.de

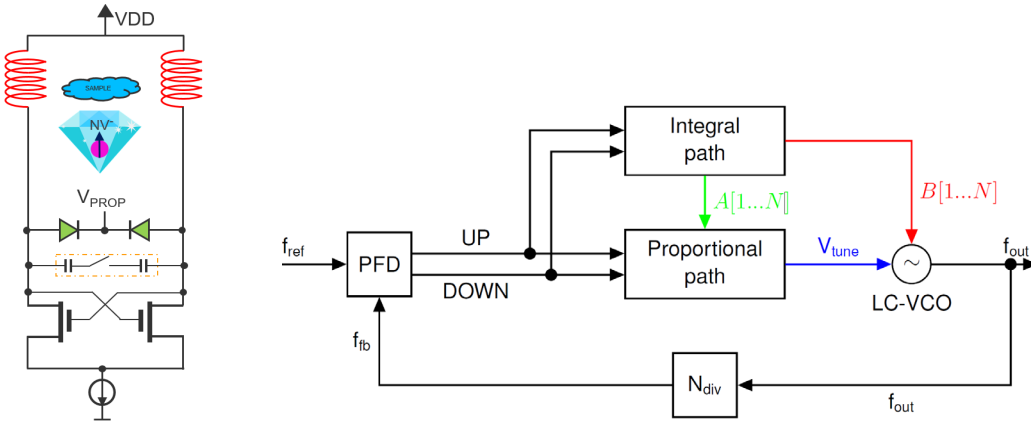

Figure 1: (a) LC VCO (b) Semi Digital PLL Block Diagram