Universität Stuttgart
Institut für Intelligente Sensorik und
Theoretische Elektrotechnik

Master's Thesis – Developing fast and low PSR low-dropout (LDO) linear voltage regulator for high-speed photonic's TIA/ ADC.

High-performance low dropout regulators (LDOs) are essential components in system-on-a-chip (SoC) designs due to their ability to provide ripple-free, fast transient response, and excellent power supply rejection (PSR) characteristics. On-chip LDOs, complemented by off-chip decoupling capacitors, are commonly employed to mitigate supply noise. However, off-chip capacitors are often ineffective in reducing supply noise at the point-of-load due to the bond-wire effect. Therefore, fully integrated, area-efficient LDOs are highly desirable for point-of-load power delivery and multi-voltage systems. Additionally, supplying power to individual noise-sensitive and/or noise-generating building blocks with separate LDOs can significantly enhance system performance. As an example, an optical receiver is shown below, *selected with green color*. A fast LDO provides a stable supply for the front-end, low-noise TIA.

In this thesis, you will design the schematic and draw the layout of an LDO linear voltage regulator using CADENCE software. The input voltage is around 1.5 V while output voltage/current equals 1V@2mA along with PSR<-40dB at 100MHz <u>although some specifications will change over the design</u>.

Required:

- ✓ Basic knowledge of IC design.

Duration: 6 months
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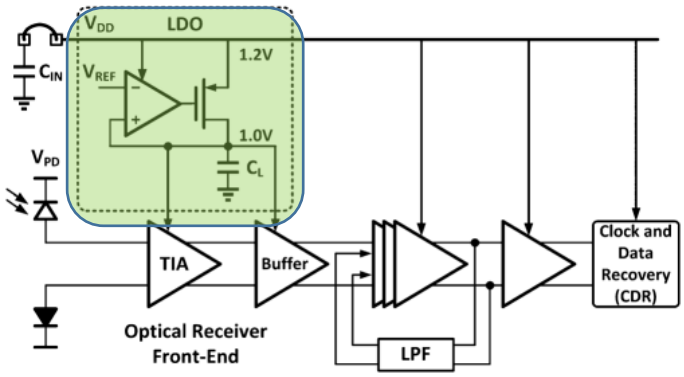

Figure1: An optical receiver with embedded LDO.